REMARKS

The Office Action of **June 14, 2002** has been received and its contents carefully noted. Applicant would like to thank the Examiner for the consideration given the present application. Concurrently filed herewith is a Request for One Month Extension of Time that extends the shortened statutory period for response to October 13, 2002. Accordingly, Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 11-20 remain pending and are believed to be in condition for allowance at least for the reasons advanced hereinbelow.

A. Objection to the Specification

The disclosure is objected to for failing to include the title "Field of the Invention." By the above action, the title "Field of the Invention" has been included. Although not objected to, the title "Description of the Related Art" was also included in order to place the disclosure in conformance with 37 C.F.R. 1.77(b). Accordingly, withdrawal of the objection is respectfully requested.

B. 35 U.S.C. 102 Rejection

Claim 1 stands rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,049,477 to Taira. Applicant respectfully contends that the claimed invention is clearly patentably distinct over the proposed combination of references for at least the reasons advanced below.

1. Summary of the Invention

The claimed invention in accordance with claim 1 is directed generally to a method for driving a semiconductor memory including whereby a magnitude of the voltage applied between a drain and a source of a FET in the step of reading data (i.e., the magnitude of the reads voltage) is set within a range where a drain-source current of the FET increases as a drain-source voltage thereof increases.

2. Taira Fails to Teach the Claimed Invention

Taira teaches an MFS transistor and an MFMIS transistor whereby "when reading information stored in the memory cell transistor 30, a Voltage V_2 is lower than the foregoing write voltage V_1 is applied to the word line WL (gate) as indicated in FIG. 4B". Taira, however, completely fails to teach, disclose or suggest setting a magnitude of the voltage applied between the drain and the source of the field effect transistor in the step of reading a data, within the range where the drain-source current of the field effect transistor increases as the drain-source voltage of the field effect transistor increases. Therefore, Applicant respectfully requests that the Examiner provide proof that Taira teaches the aforementioned claimed feature or withdraw the rejection as lacking the necessary requirements for establishing anticipation under §102.

C. 35 U.S.C. 103 Rejection

Claim 2 stands rejected under 35 U.S.C. §103(a) as unpatentable over Taira in view of U.S. Patent No. 6,362,500 to Ishiwara. Applicant respectfully contends that the claimed invention is clearly patentably distinct over the proposed combination of references for at least the reasons advanced below.

1. Summary of the Invention

The claimed invention in accordance with claim 2 is directed generally to a method for driving a semiconductor memory including whereby a magnitude of the voltage applied between a drain and a source of a FET in the step of reading data (i.e., the magnitude of the reads voltage) is set within a range where a drain-source current of the FET increases as a drain-source voltage thereof increases. Accordingly, the lowering of the drain-source current with time can be suppressed. As a result, the data storing time, and thus the retention characteristic can be improved.

2. The Proposed Combination of References Fail to Disclose the Claimed Invention

As previously established hereinabove, Taira completely fails to teach setting a magnitude of the voltage applied between the drain and the source of the field effect transistor in the step of reading a data, within the range where the drain-source current of the field effect transistor increases as the drain-source voltage of the field effect transistor increases.

The secondary reference Ishiwara fails to modify the aforementioned deficiency in Taira

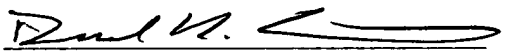
in a manner that renders claim 2 *prima facie* obvious. For instance, while Ishiwara teaches at column 5, lines 44-49 a method "comprising the steps of setting the other electrode of the second ferroelectric capacitor into an electrically floating state; applying a positive voltage pulse on the other electrode of the first ferroelectric capacitor; and subsequently applying a negative voltage pulse whose absolute value is smaller than the positive voltage pulse to the other electrode of the first ferroelectric capacitor," Ishiwara lacks a method that includes setting a magnitude of the voltage applied between the drain and the source of the field effect transistor in the step of reading a data, within the range where the drain-source current of the field effect transistor increases as the drain-source voltage of the field effect transistor increases. Thus, the combined combination of Taira and Ishiwara fails to achieve the claimed invention. Insofar as the combined references fail to achieve the claimed invention, the non-obvious advantages that result from claim 2, namely, suppression of the lowering of the drain-source current with time to thereby enhance the data storing time, and enhancing the retention characteristic.

Therefore, Applicant respectfully requests that the Examiner provide proof that Taira and/or Ishiwara provides a direct teaching, disclosure or suggestion of the aforementioned claimed feature or withdraw the rejection as lacking the necessary requirements for establishing *prima facie* obviousness under §103.

CONCLUSION

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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